

FIG. 1A

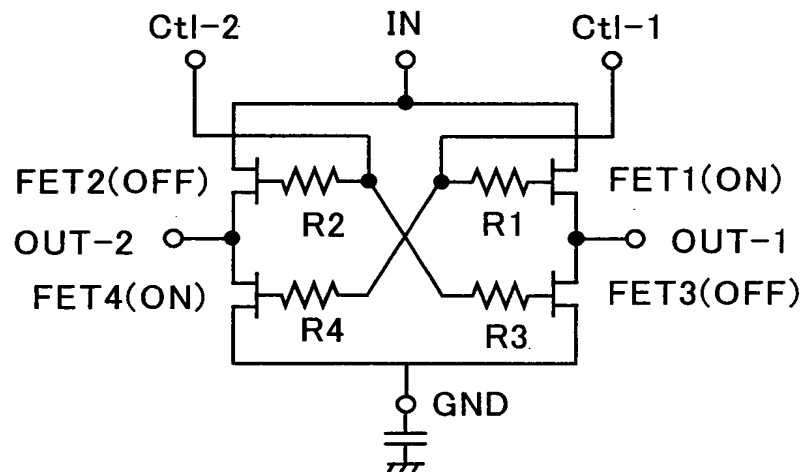


FIG. 1 B

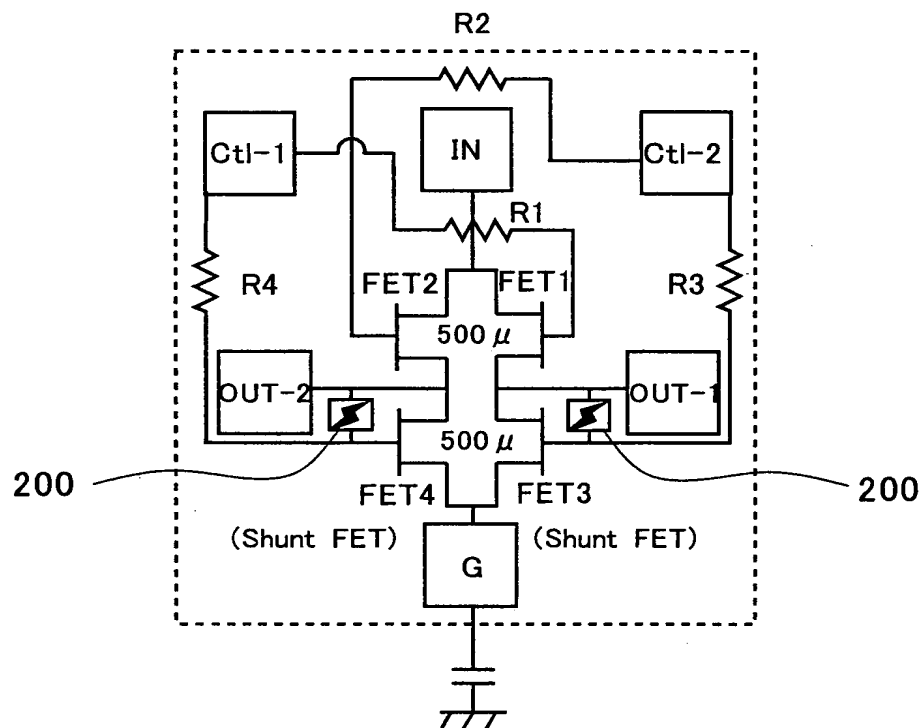


FIG.2

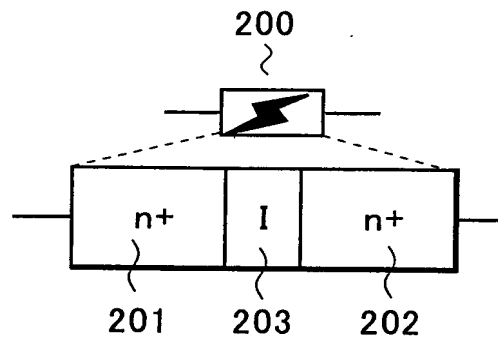


FIG.3A

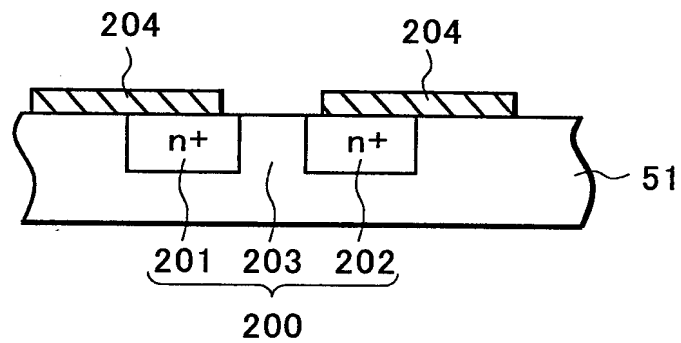
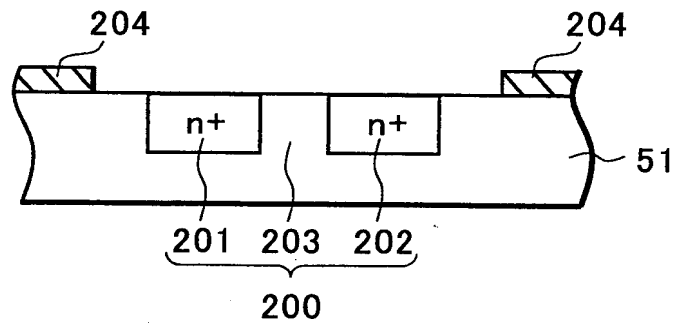
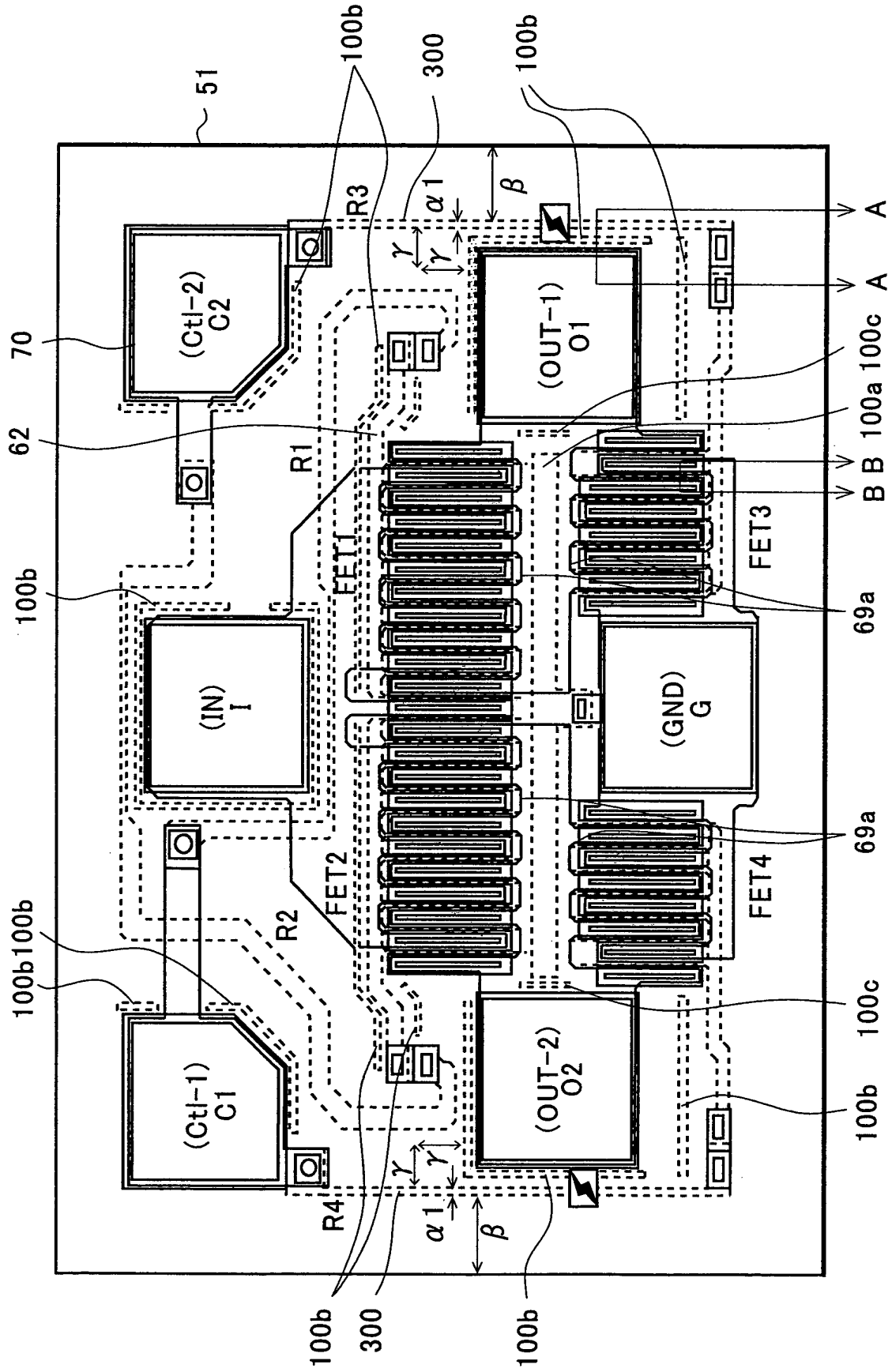


FIG.3B



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FIG.4



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FIG.5

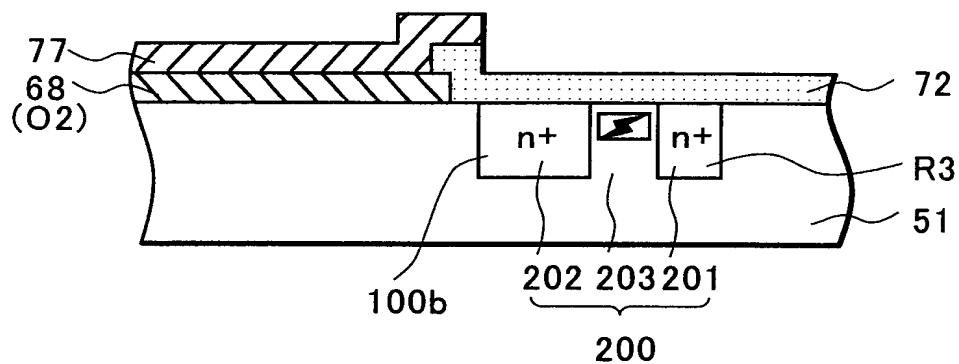


FIG.6A

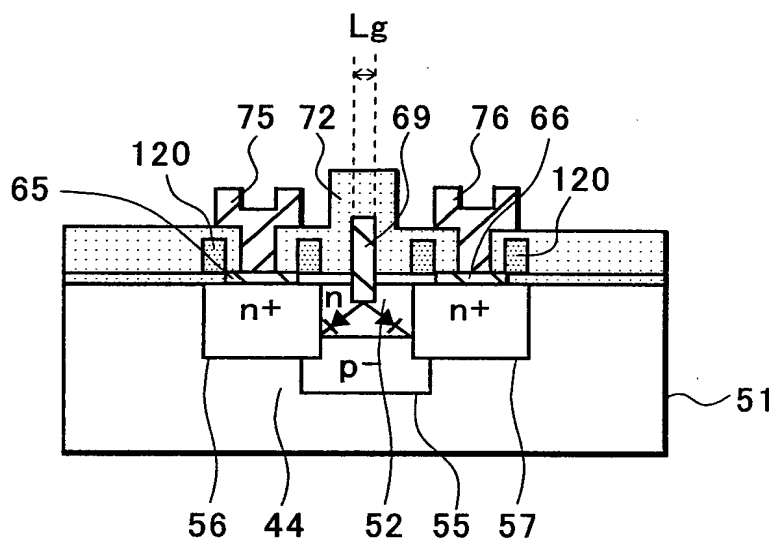


FIG.6B

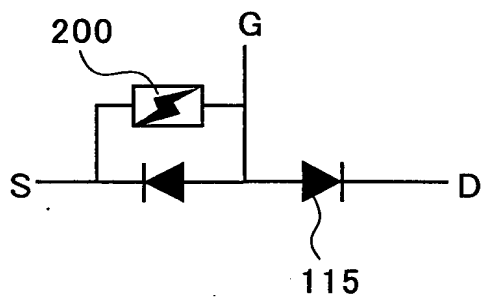
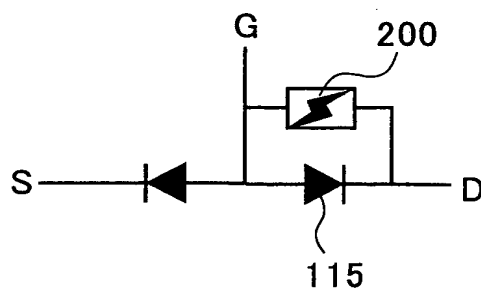


FIG.6C



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FIG. 7

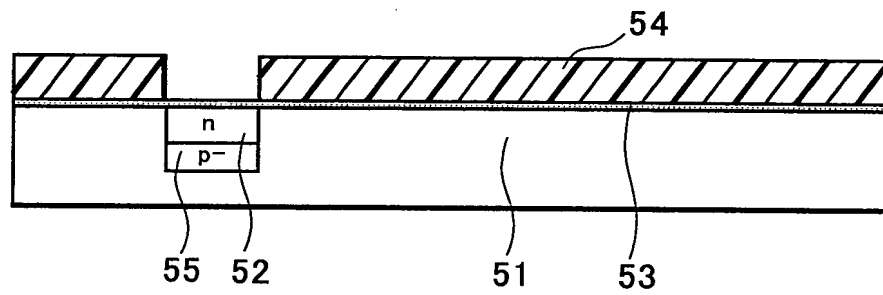


FIG. 8

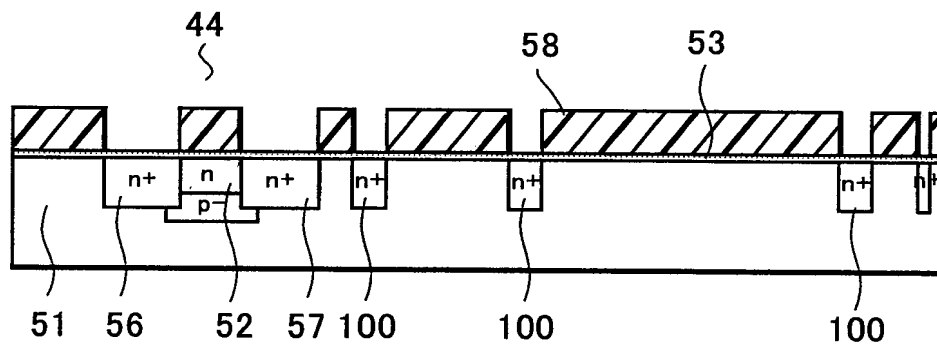


FIG.9A

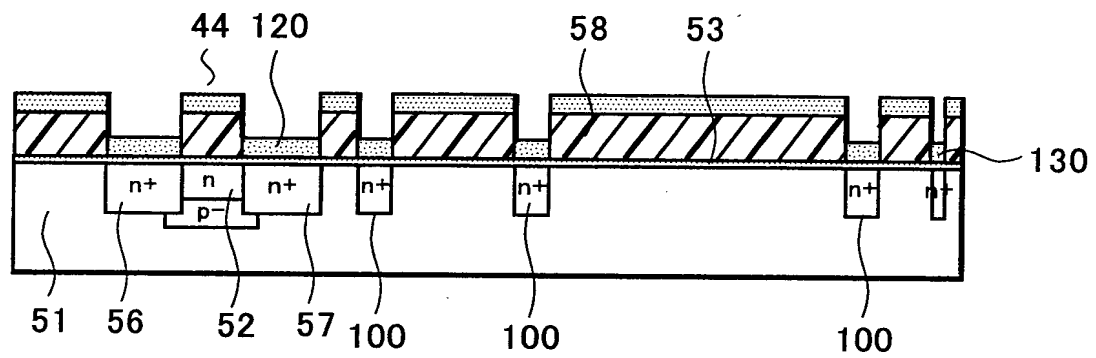
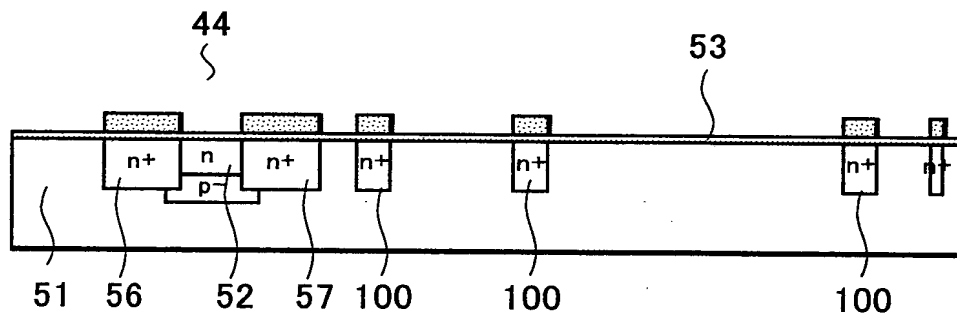


FIG.9B



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FIG.10A

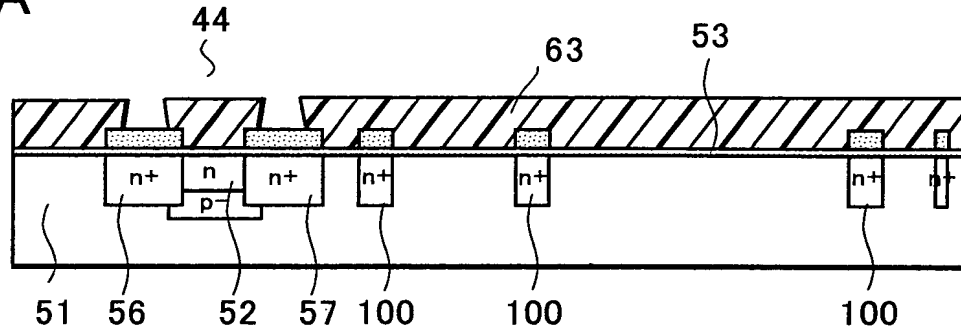


FIG.10B

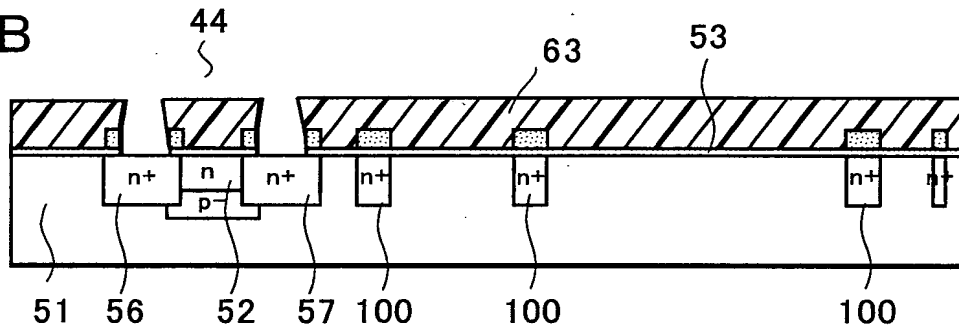


FIG.10C

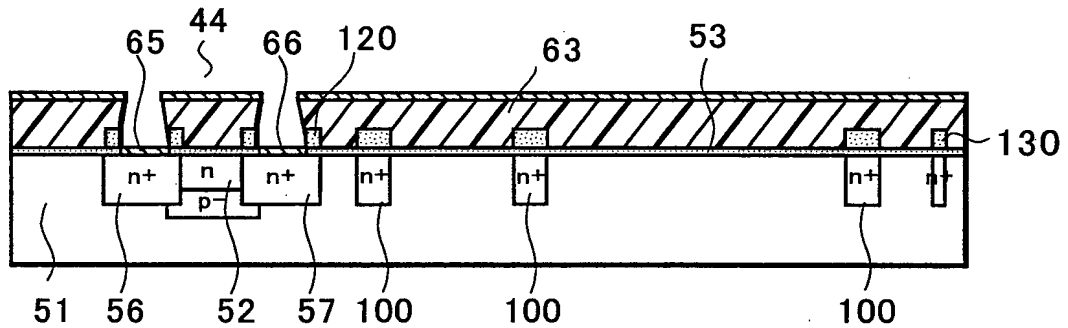
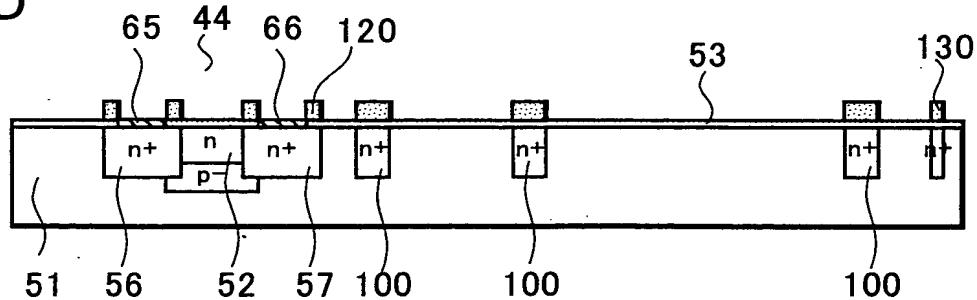


FIG.10D



This cross-sectional view shows a semiconductor device with a substrate. A series of regions are formed on the surface, including regions labeled 56, 52, 57, and 100. Region 56 contains an n+ layer, region 52 contains an n layer and a p layer, region 57 contains an n+ layer, and region 100 contains an n+ layer. A gate structure 67 is positioned over the central part of the device.

A cross-sectional view of a semiconductor device. The device features a substrate with a series of gates (56, 52, 57, 100, 100, 100) and contacts (69, 62, 70, 68). The gates are formed on a p-type region (p-) and are separated by n+ regions. The contacts are formed on the n+ regions. The device is covered by a protective layer (67) and a passivation layer (68). The gates are labeled 56, 52, 57, 100, 100, 100. The contacts are labeled 69, 62, 70, 68. The p-type region is labeled p-. The n+ regions are labeled n+. The protective layer is labeled 67. The passivation layer is labeled 68.

A cross-sectional view of a semiconductor device 100. The device is built on a substrate 56. It features a series of n+ regions (52, 57, 100) separated by p- regions (52, 57). A central region 70 is shown with a hatched pattern. A gate structure 62 is positioned over the central region 70. A contact pad 69 is located on the left side of the device.

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FIG.12A

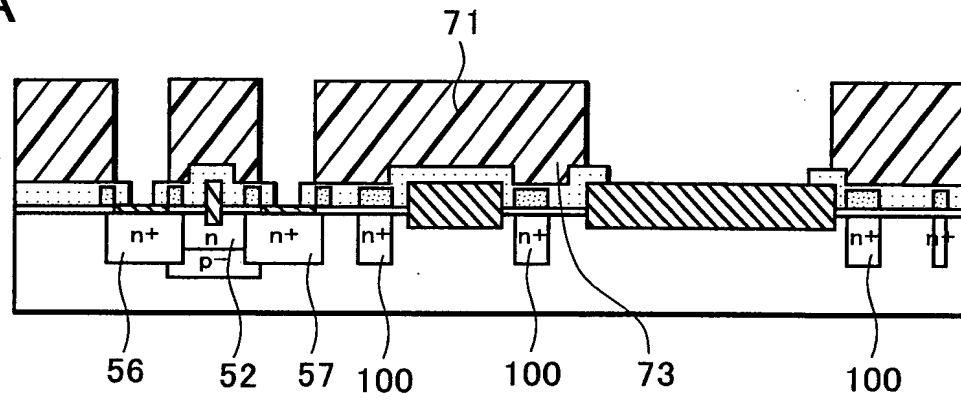


FIG.12B

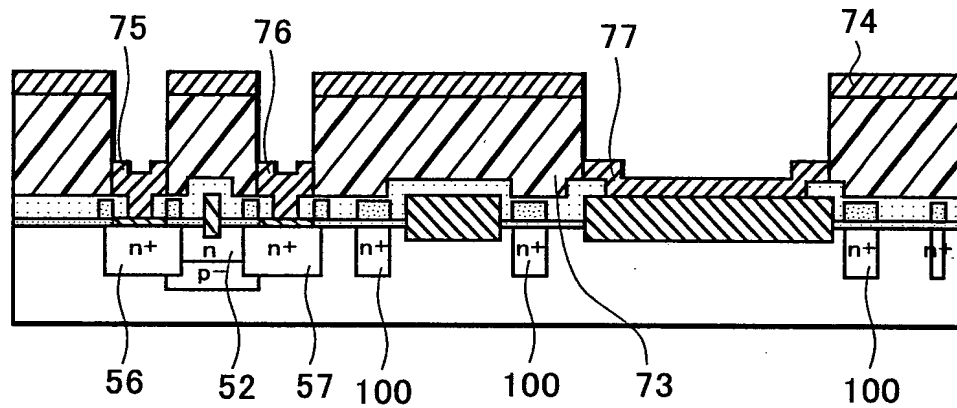


FIG.12C

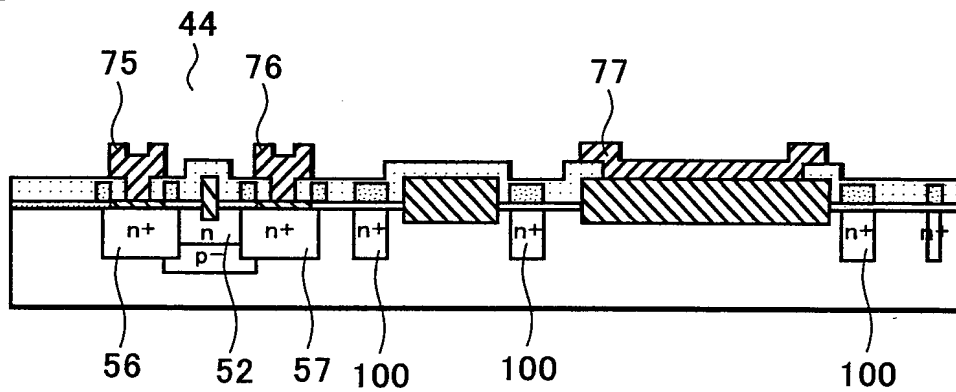
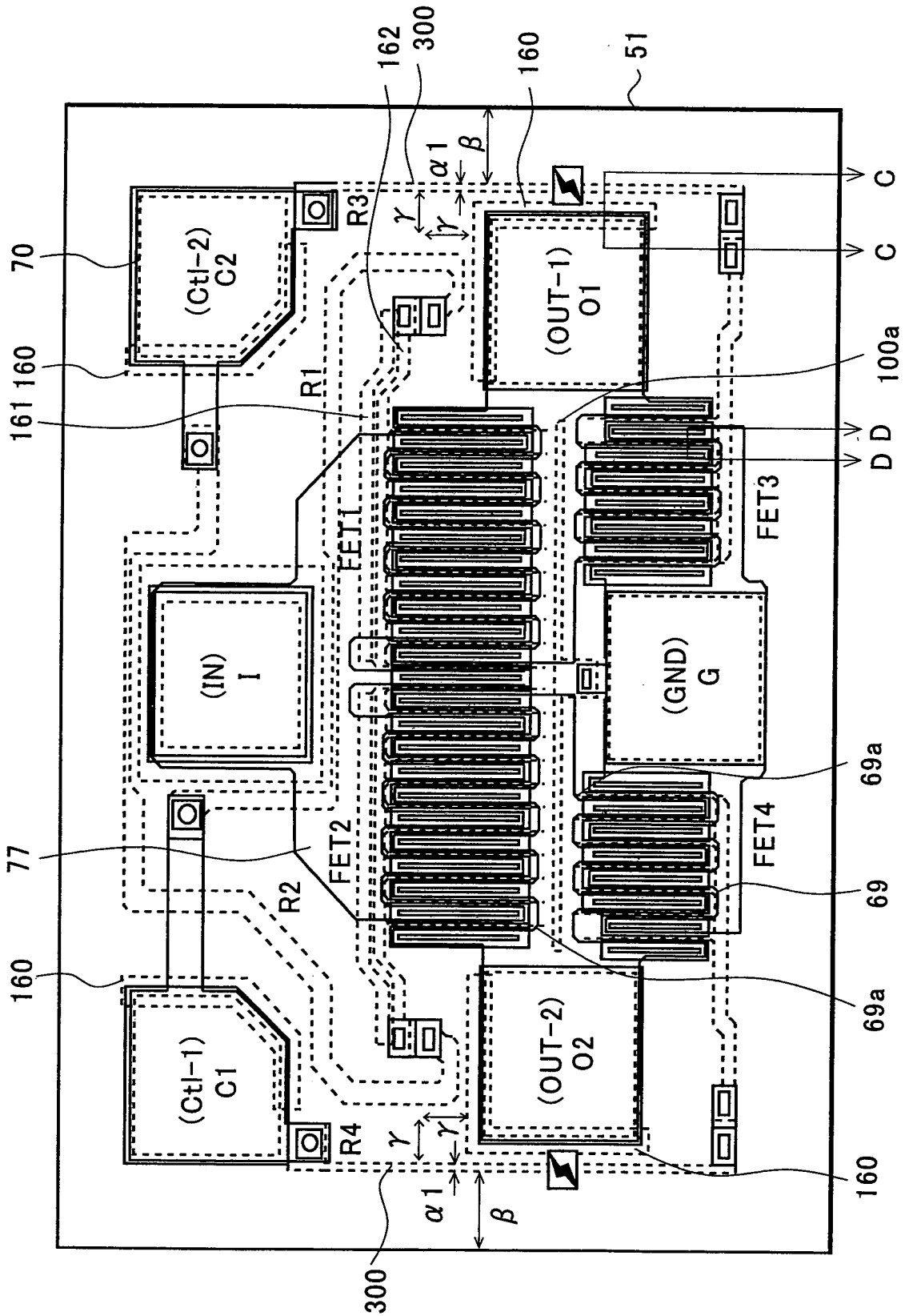


FIG. 13



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FIG.14A

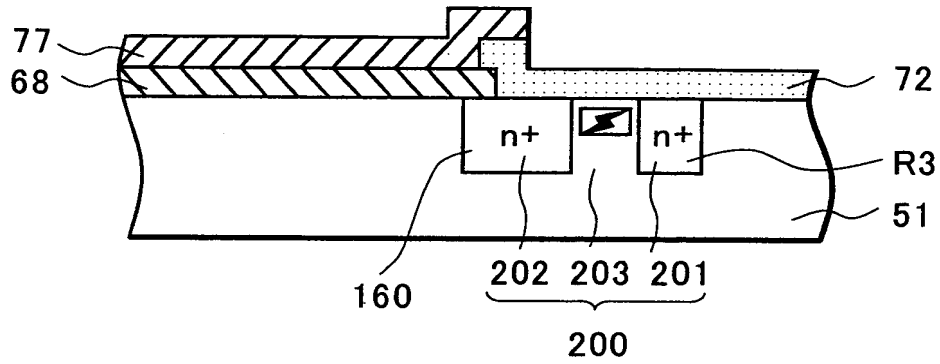


FIG.14B

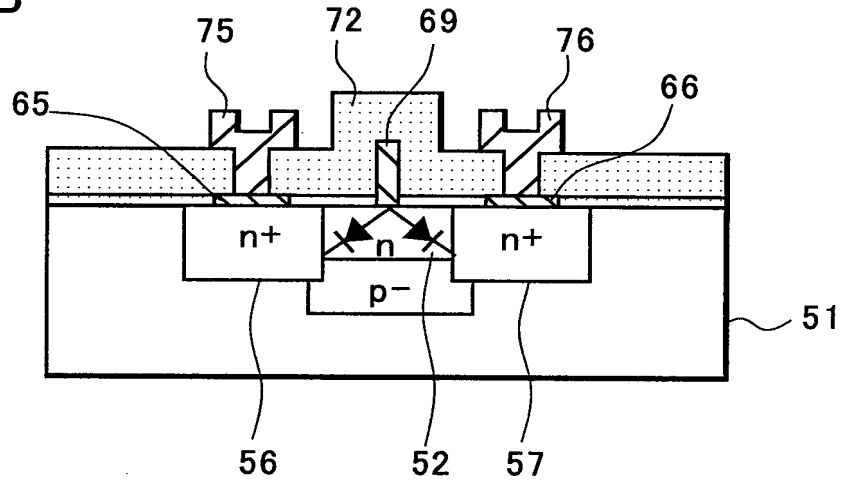


FIG.14C

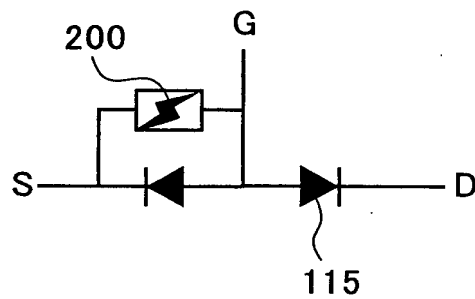
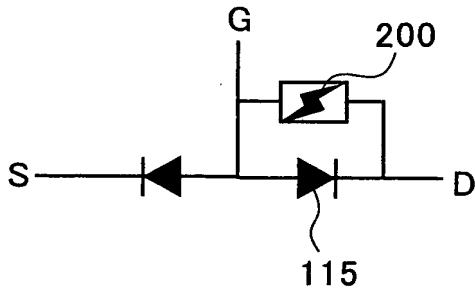


FIG.14D



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FIG.15

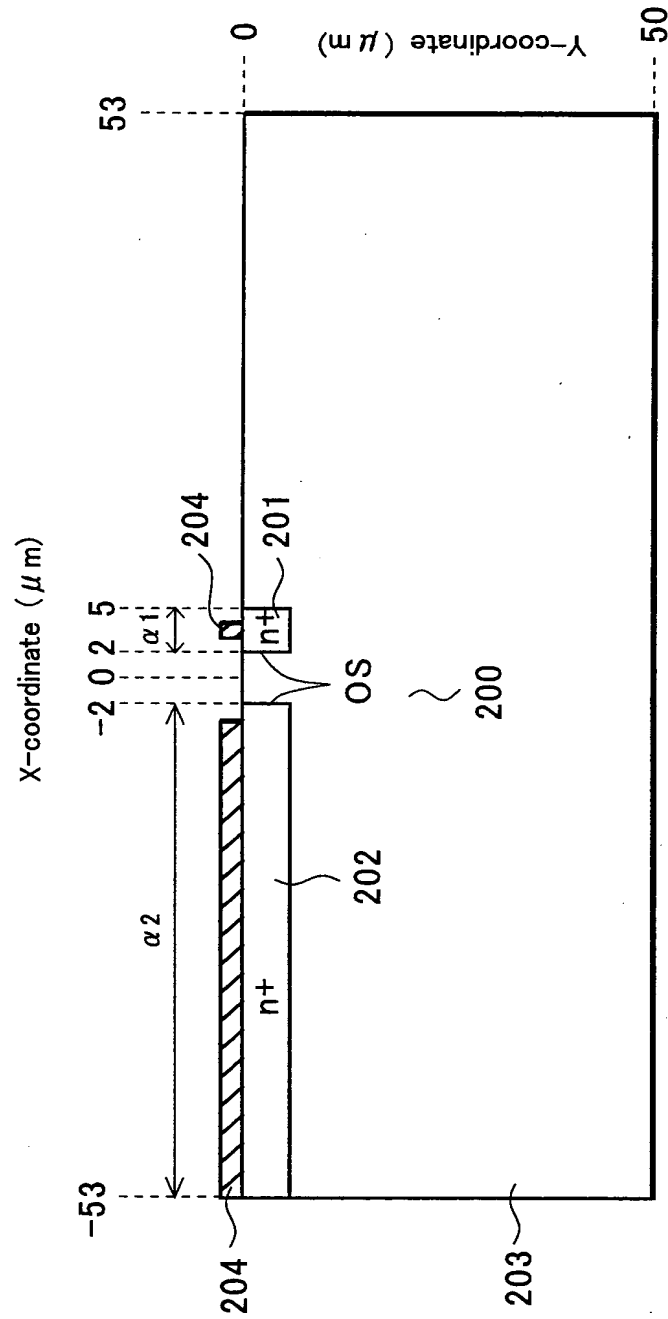


FIG. 16

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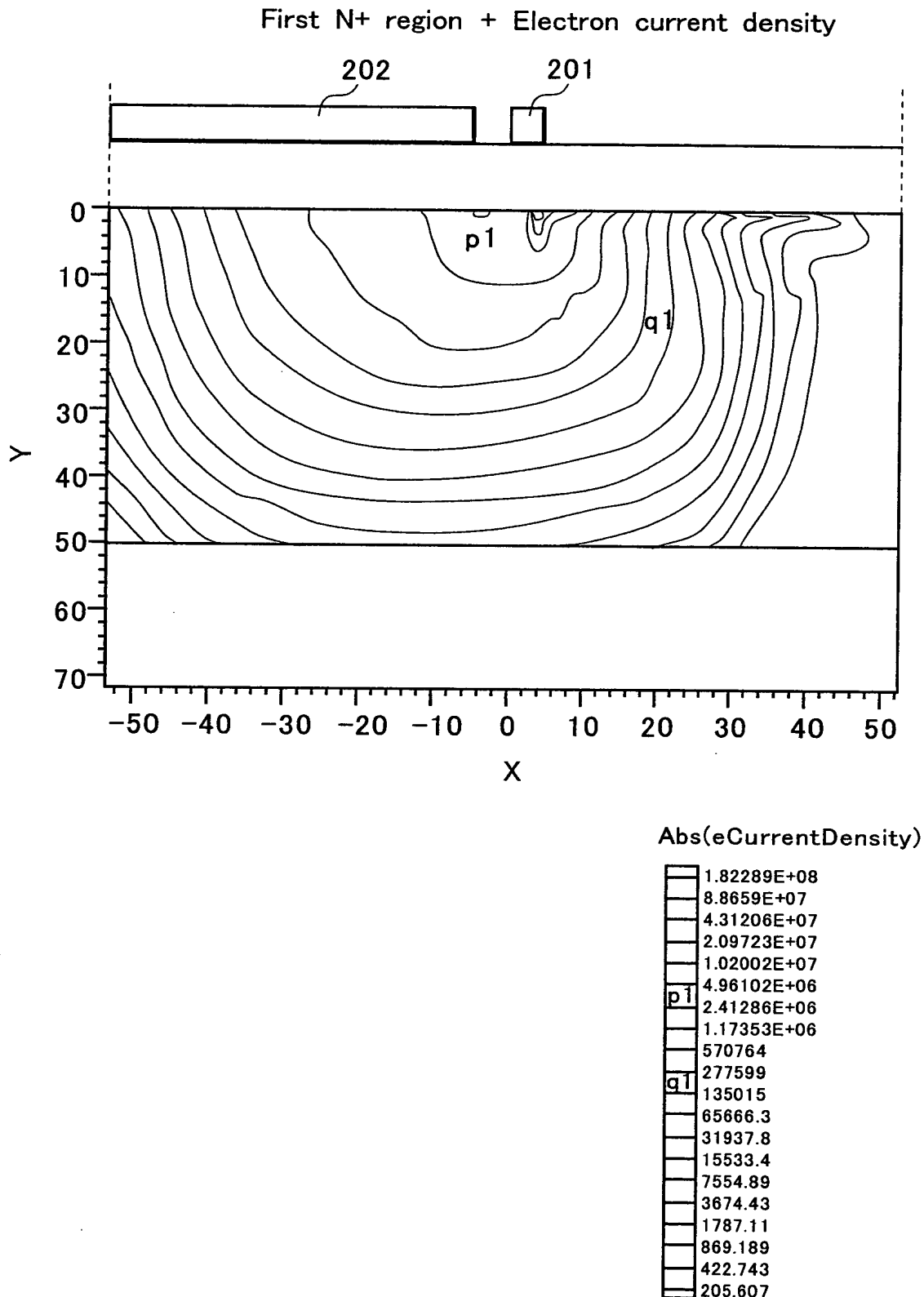


FIG.17

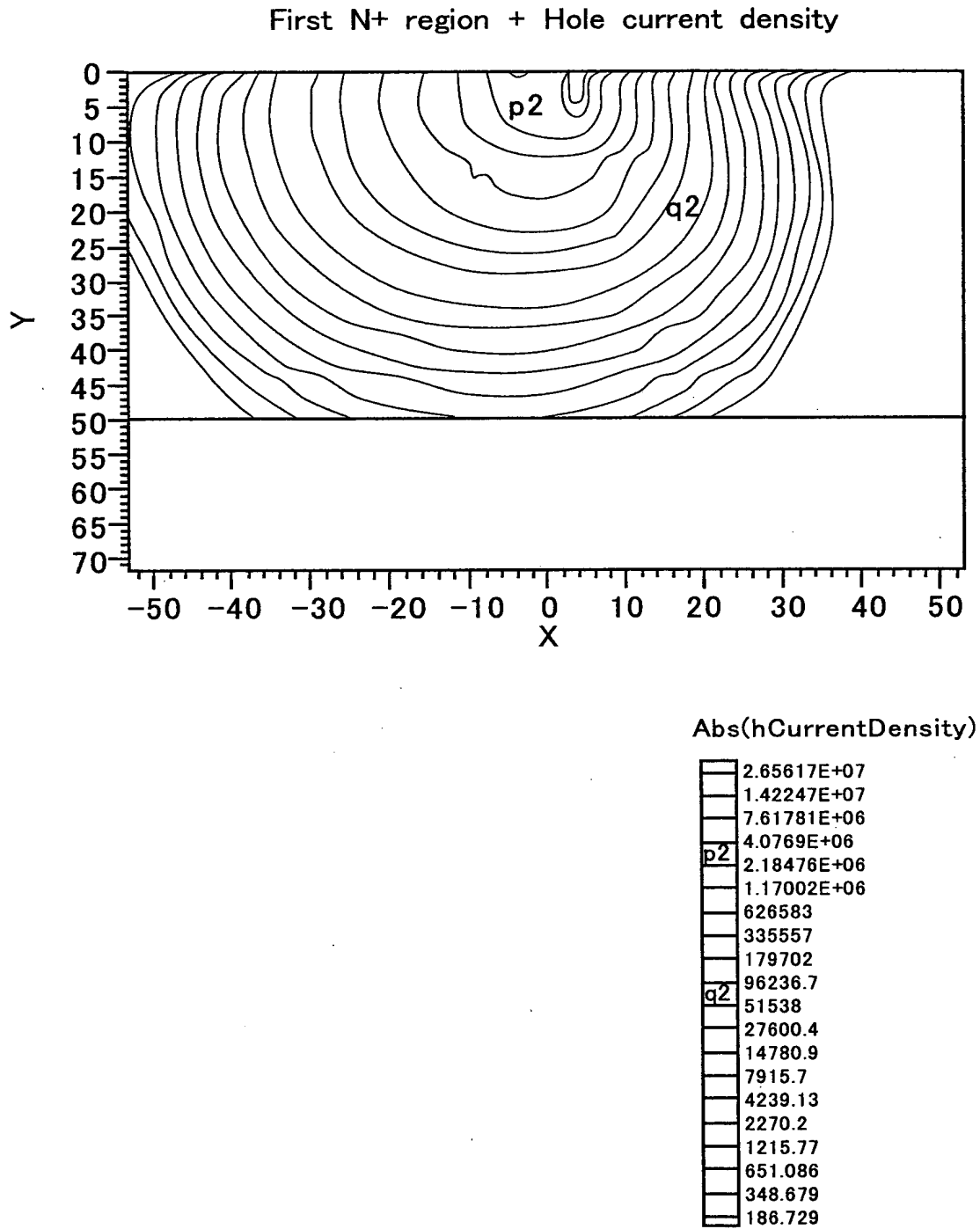
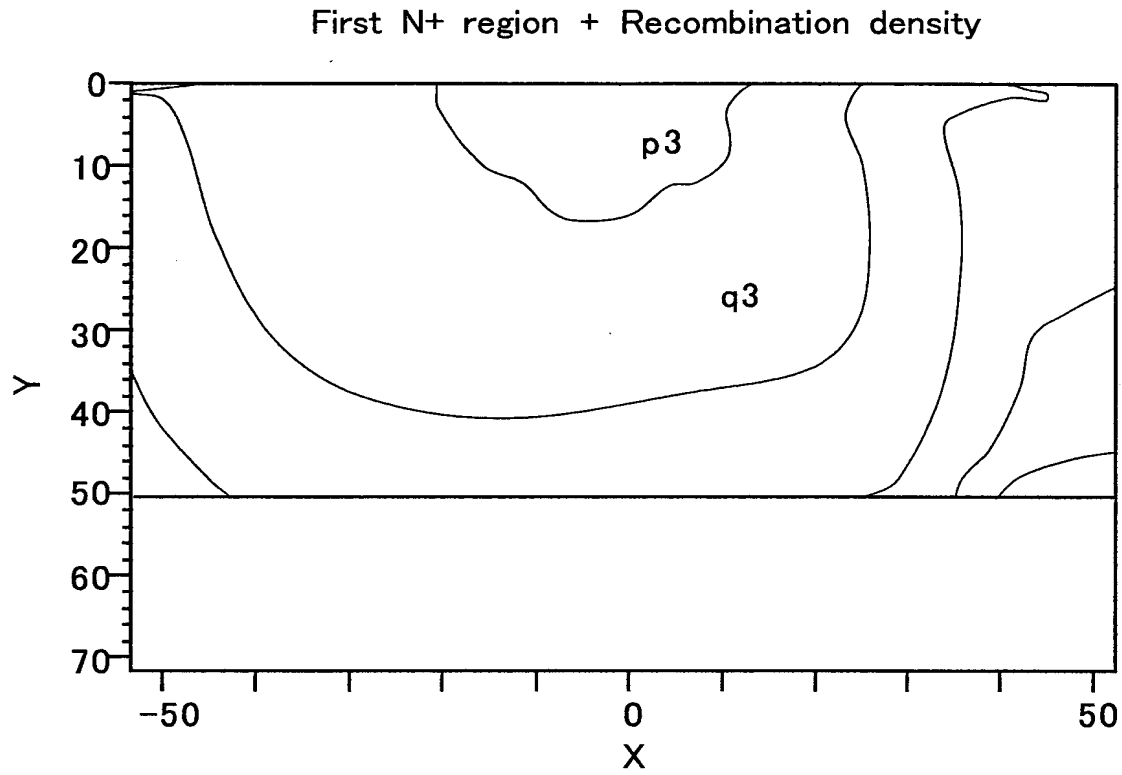


FIG.18

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srhRecombination

	3.79523E+29
	1.5859E+28
p3	6.62696E+26
q3	2.76919E+25
	1.15715E+24
	4.83536E+22
	2.02054E+21
	8.44316E+19
	3.52812E+18
	1.47428E+17
	6.16055E+15
	2.57429E+14
	1.07571E+13
	4.49504E+11
	1.87833E+10
	7.84892E+08
	3.2798E+07
	1.37052E+06
	57269.6
	2393.11

FIG.19A

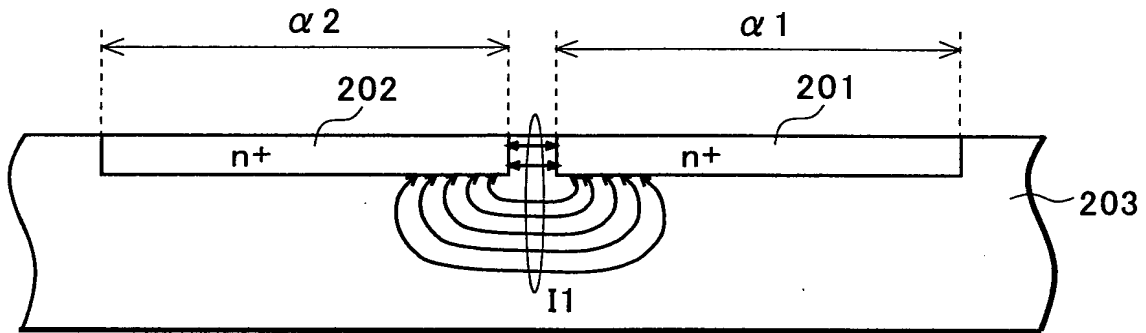


FIG.19B

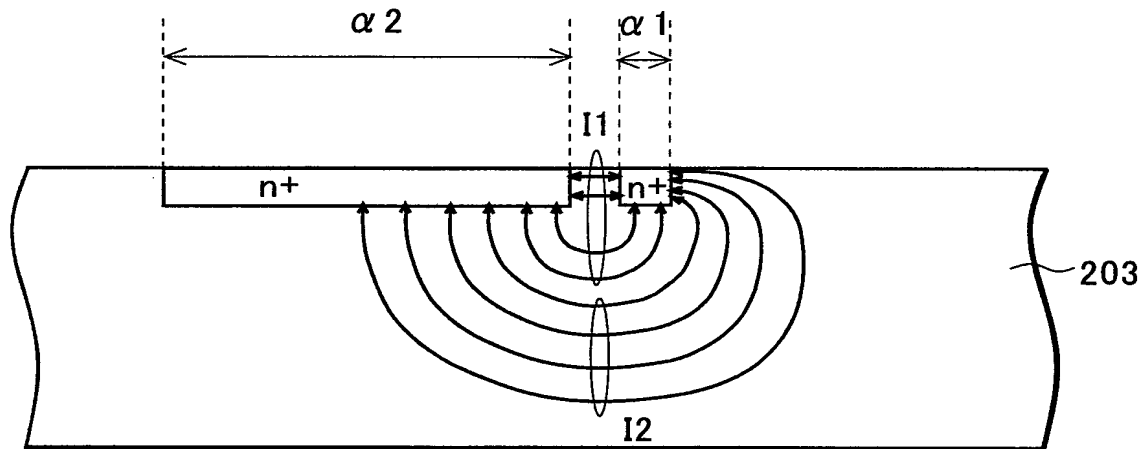


FIG.20

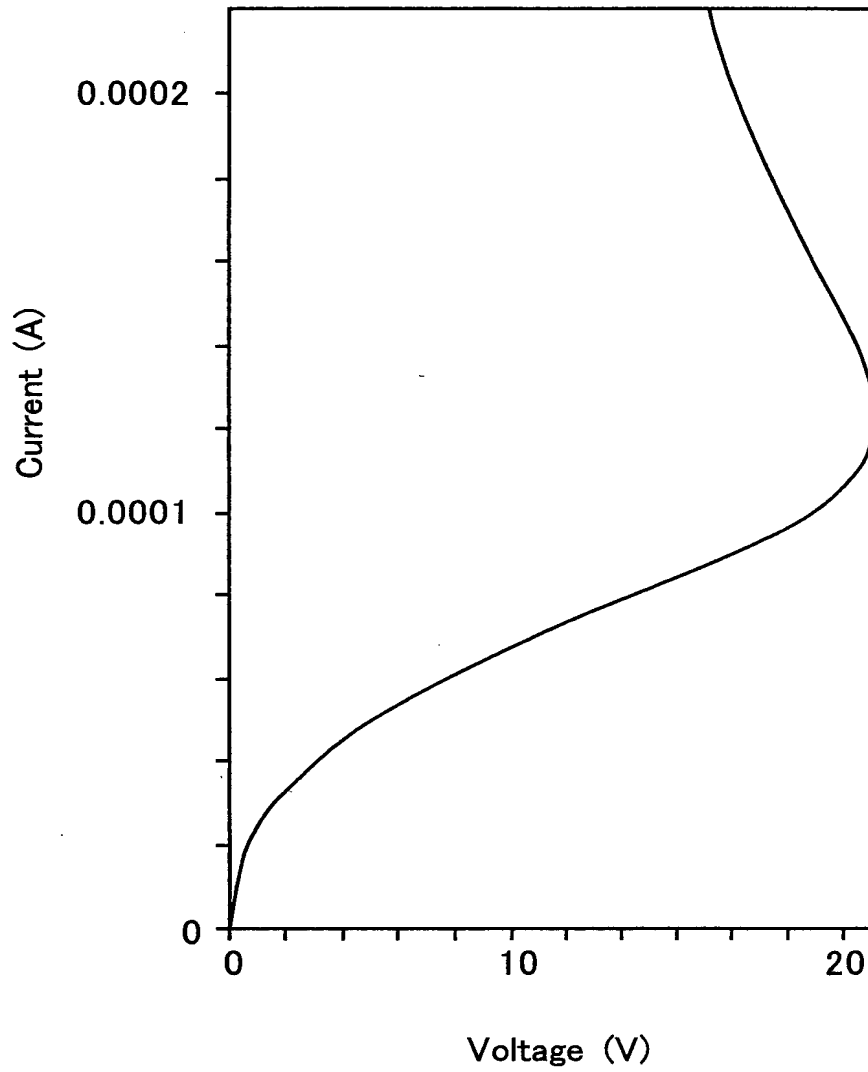


FIG.21

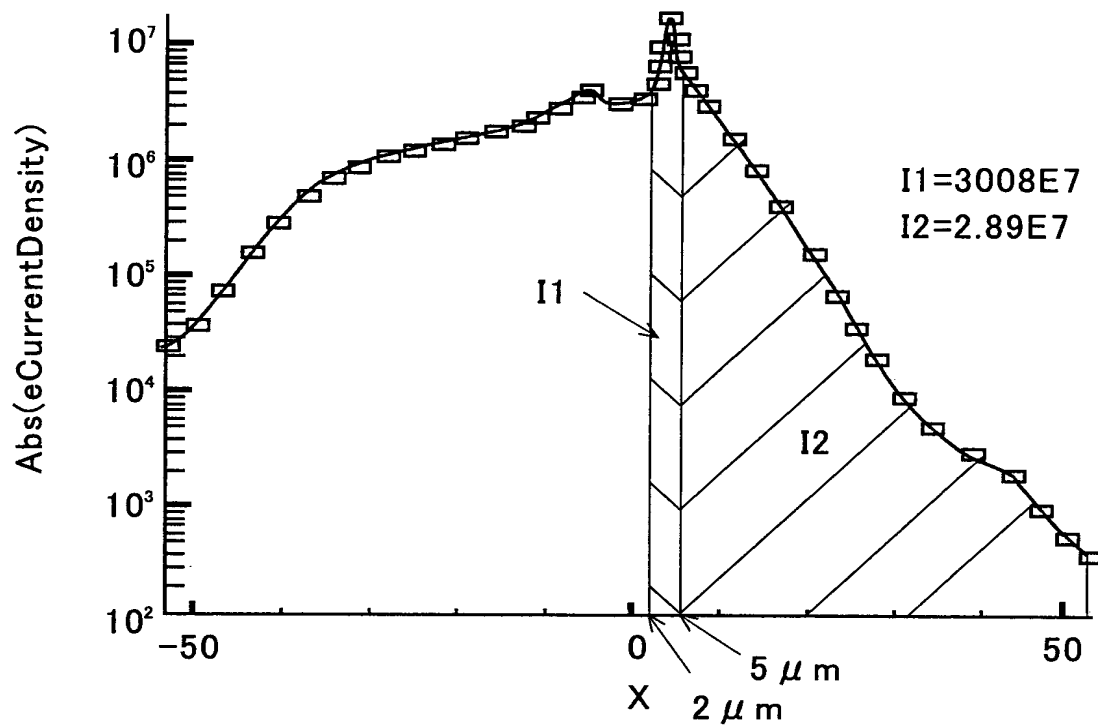


FIG.22A

Comparison of spreading of currents and recombination

	a-structure			b-structure-1			b-structure-2		
Electron current density	y__2	x__0	Product	y__2	x__0	Product	y__2	x__0	Product
	21.9	10.5	230.0	26	15	390.0	23.8	11.3	268.9
Hole current density	y__2	x__0		y__2	x__0		y__2	x__0	
	13.7	6	82.2	23.9	12.5	298.8	12.7	7.4	94.0
Recombination density	y__2	x__0		y__2	x__0		y__2	x__0	
	29.7	14.8	439.6	33.1	20	662.0	33.9	15.5	525.5

FIG.22B

b-structure-3		
y__2	x__0	Product
69	36.1	2490.9
y__2	x__0	
47.9	29.1	1393.9
y__2	x__0	
80 or more	43.9	3512 or more

FIG.22C

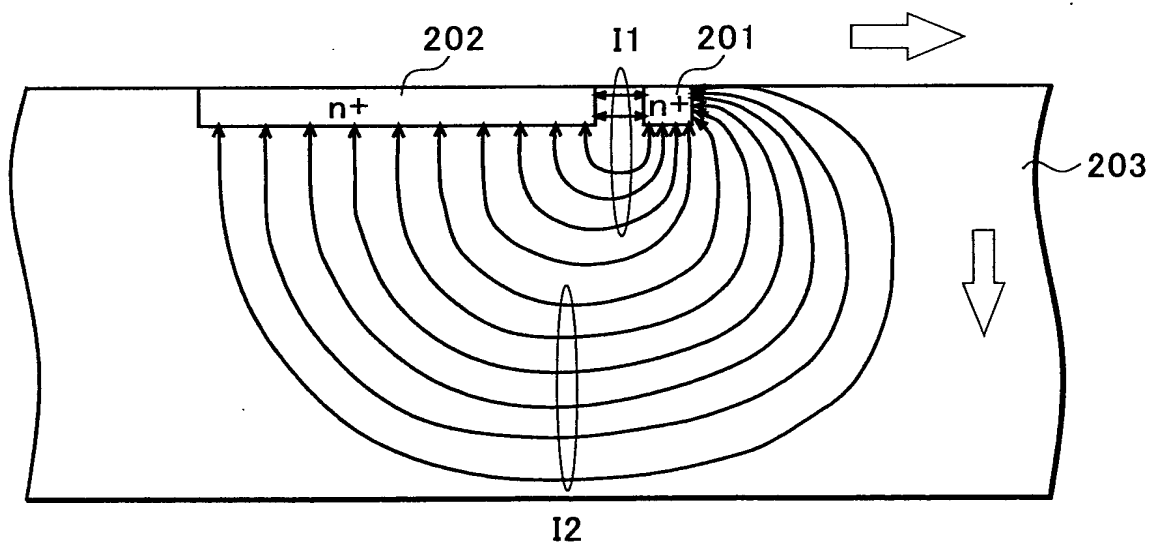
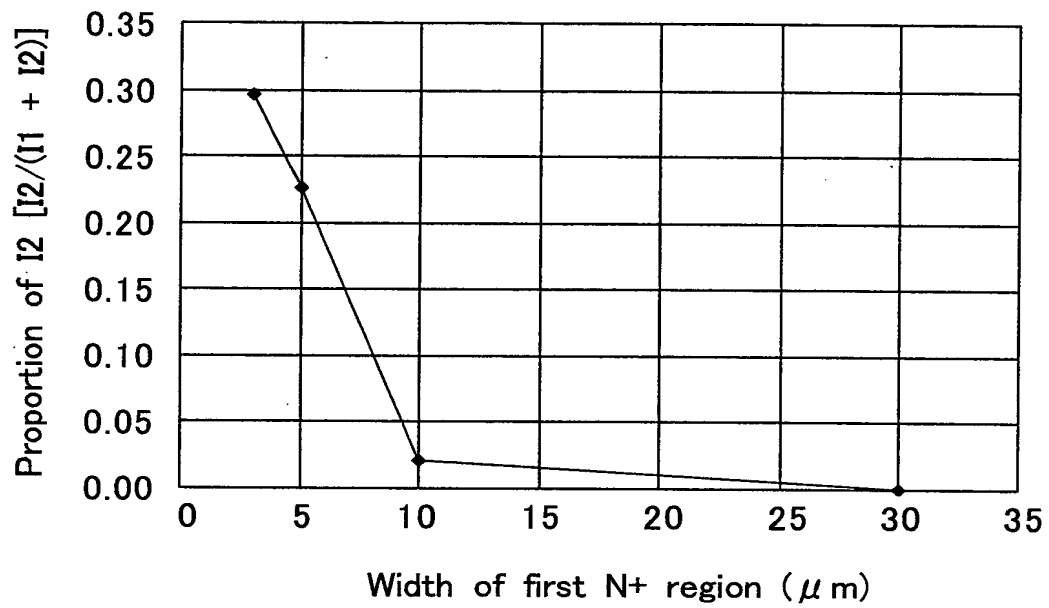


FIG.23

Relationship between the proportion of I2
and the width of the first N+ region



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FIG.24A

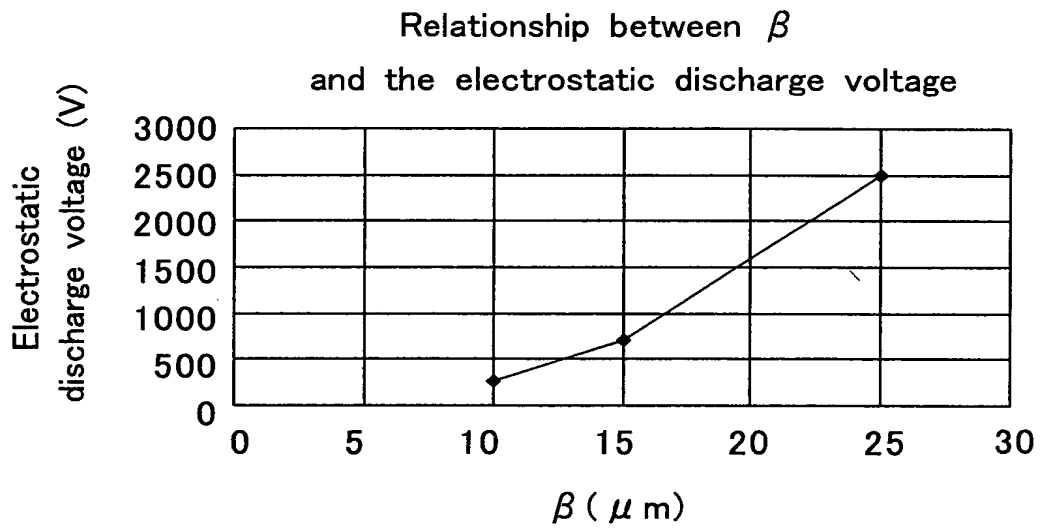
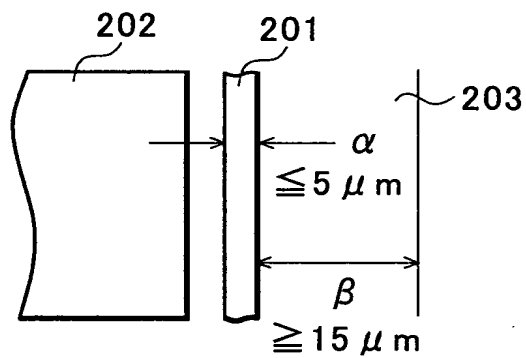


FIG.24B



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FIG.25A

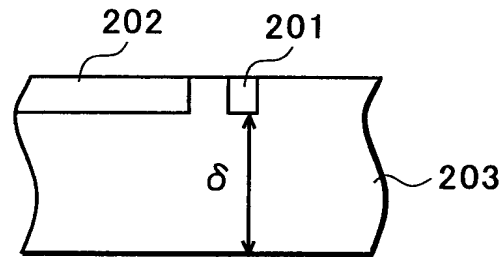


FIG.25B

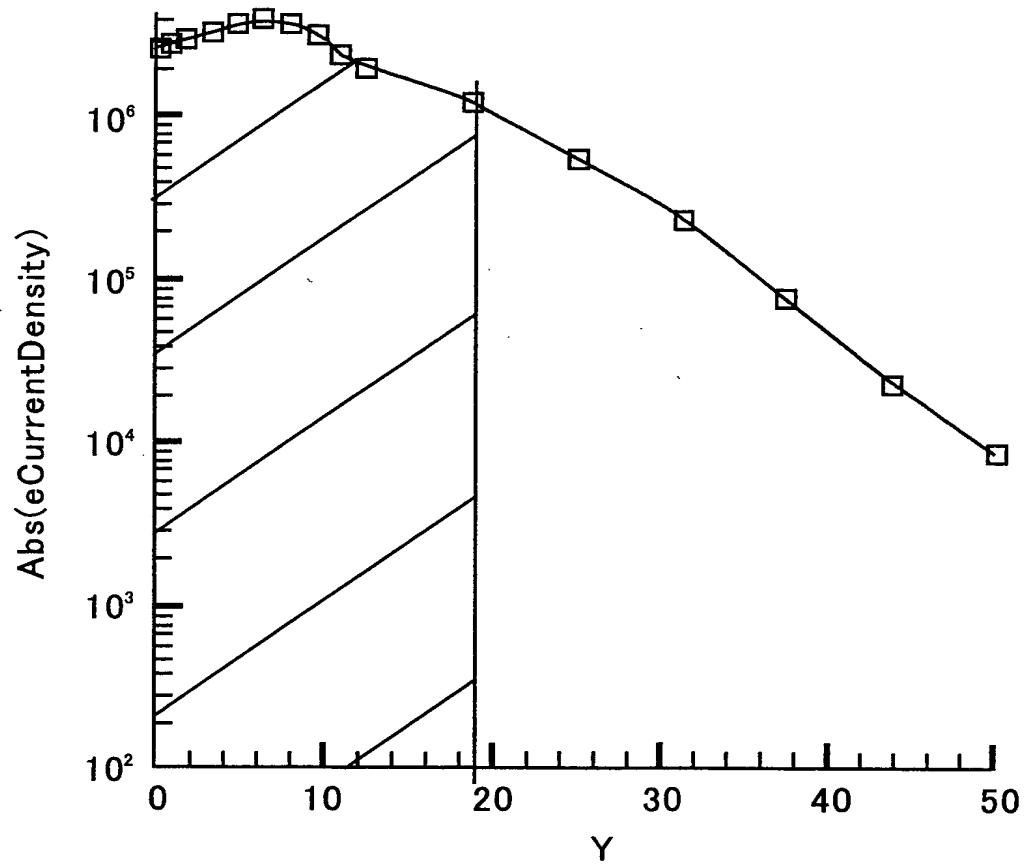
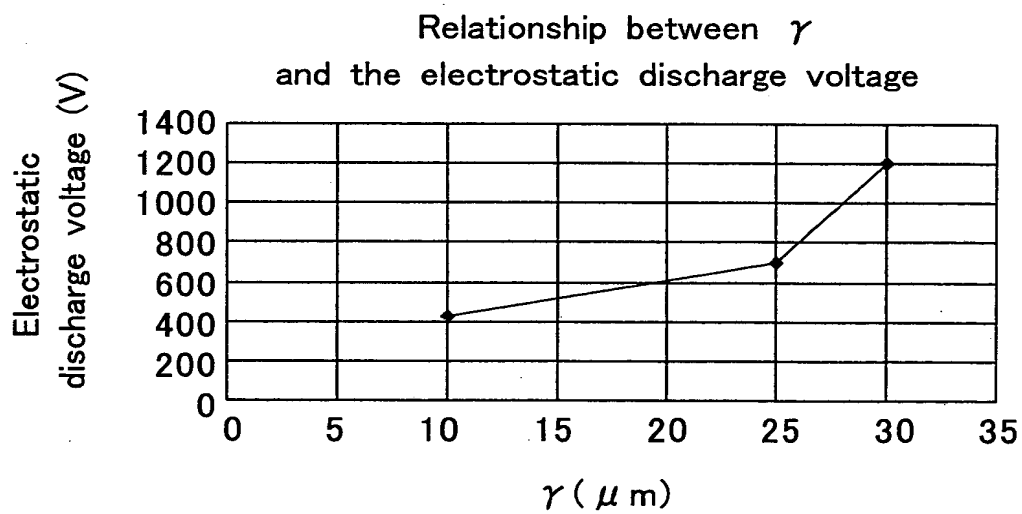


FIG. 26B



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FIG.27

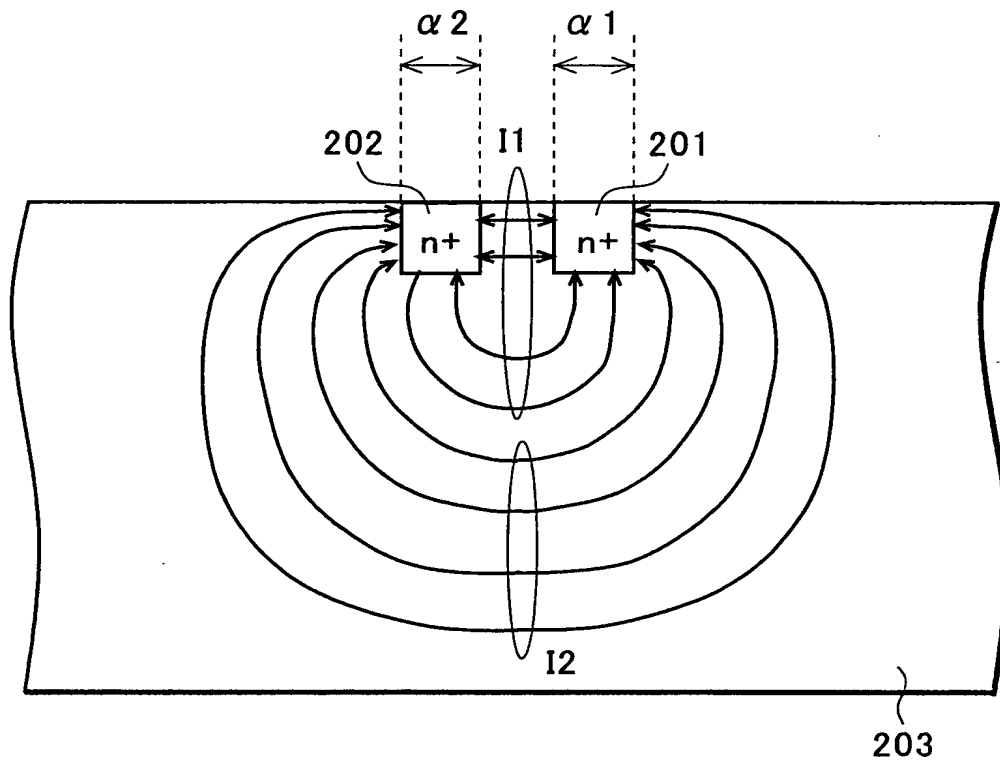
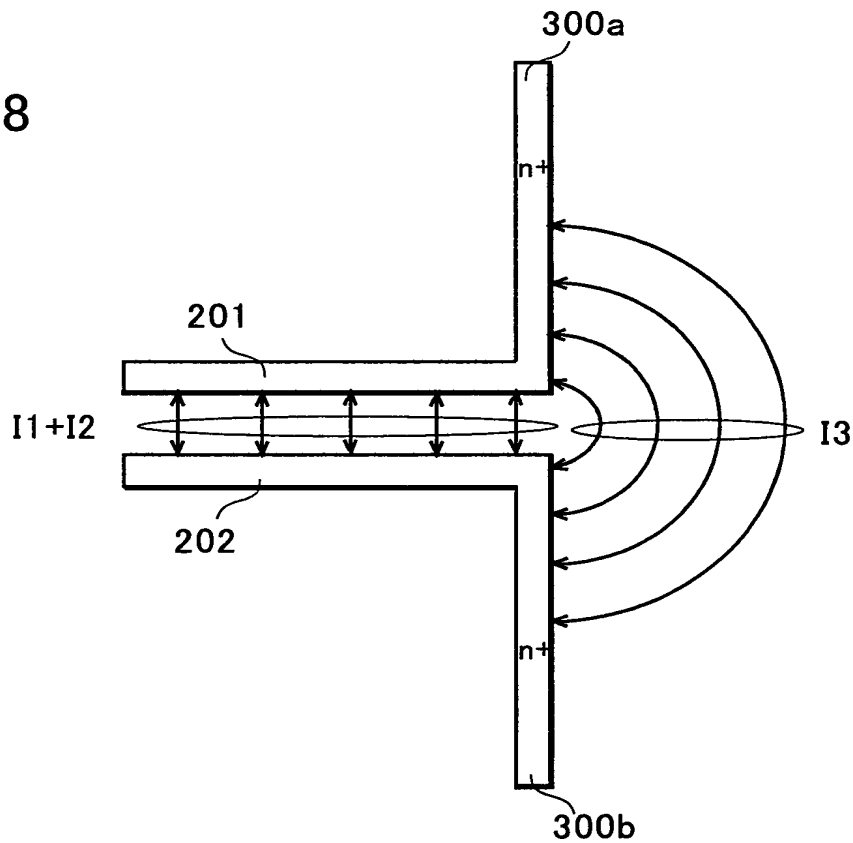
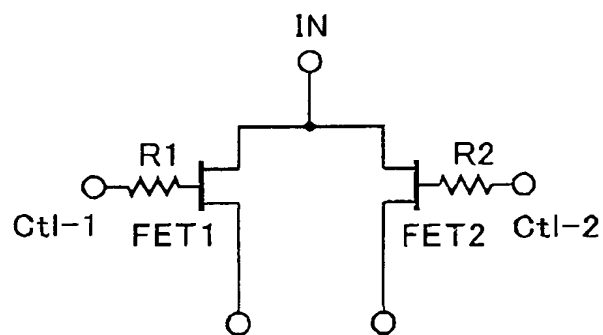


FIG.28



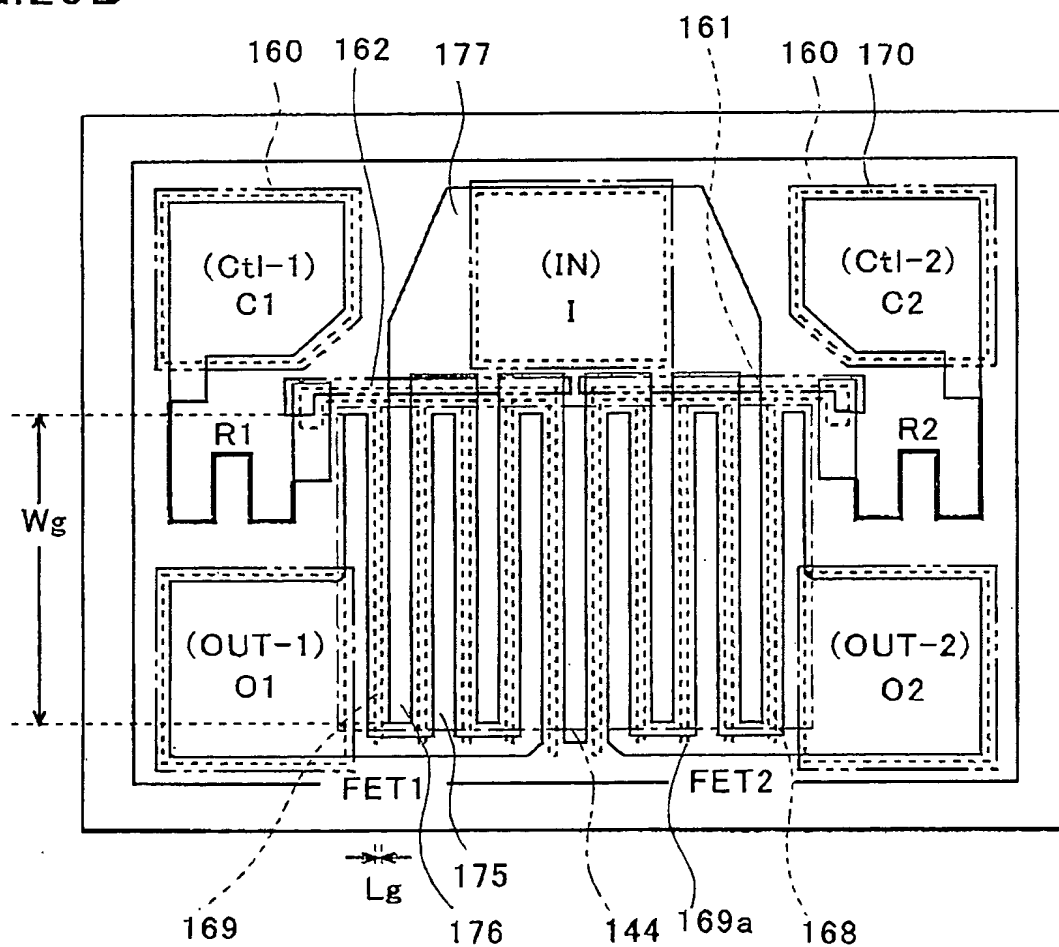
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FIG.29A



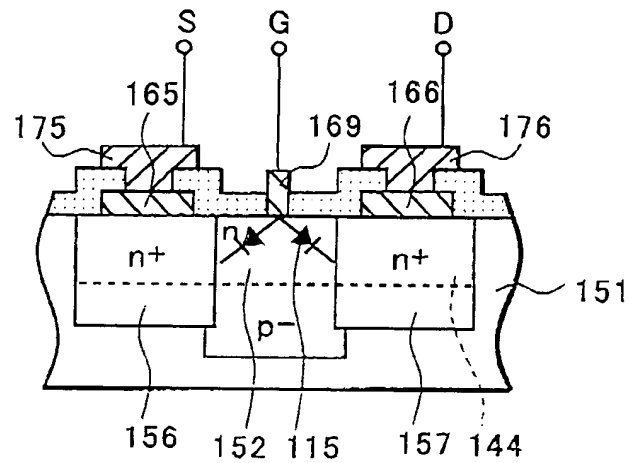
Prior Art

FIG.29B



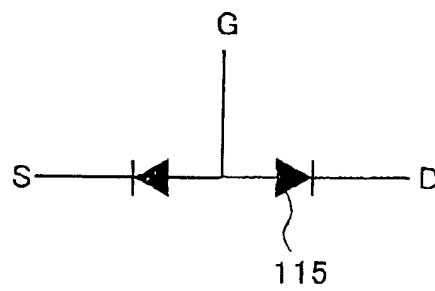
Prior Art

FIG.30A



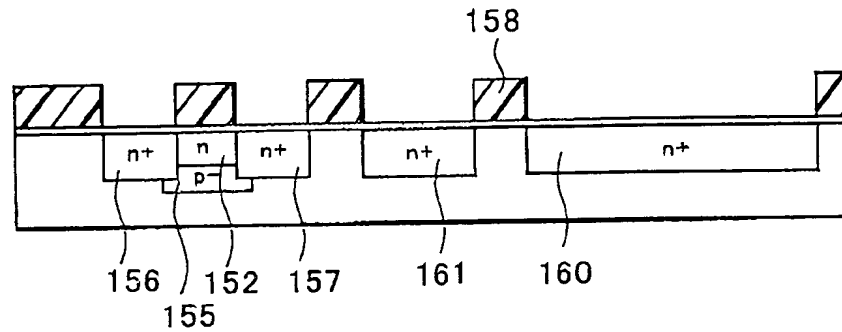
Prior Art

FIG.30B



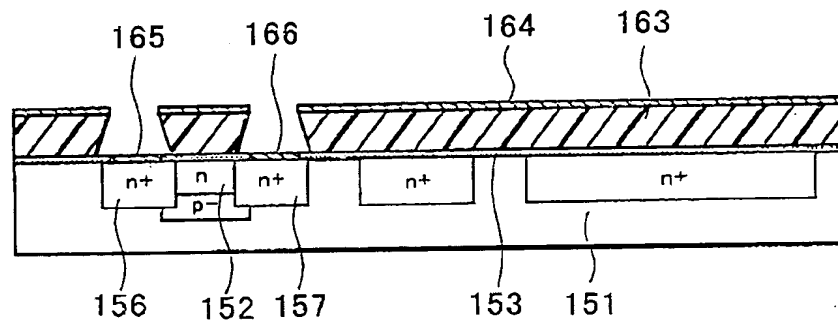
Prior Art

FIG.31A



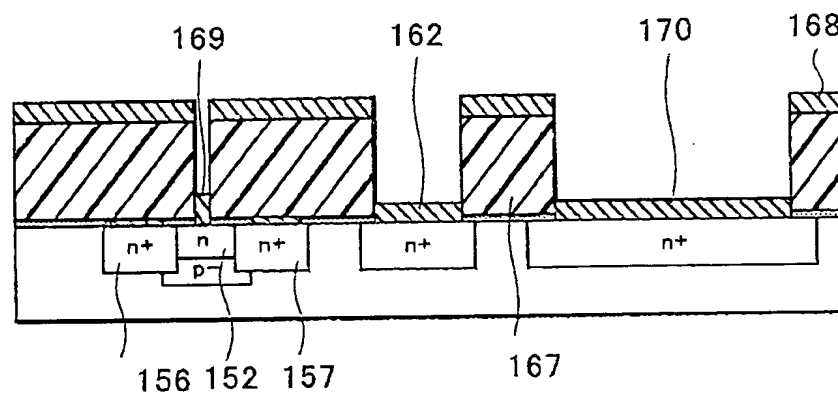
Prior Art

FIG.31B



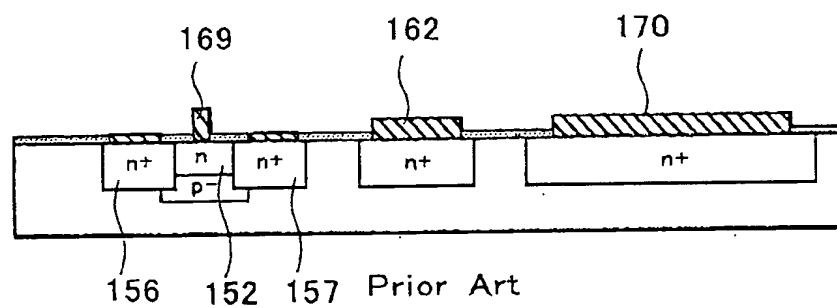
Prior Art

FIG.31C



Prior Art

FIG.31D



Prior Art

This diagram shows a cross-sectional view of a prior art semiconductor device. It features a substrate with a p-type region (155) and n+ regions (156, 157, 172). A central n-type region (152) is shown with a p+ region (153) on top. A gate structure (171) is positioned over the central region. The device is shown with various layers and regions labeled with numbers and symbols.

This diagram shows a cross-sectional view of a semiconductor device in the prior art. It features a substrate with a p-type region (p-) and n+ regions. A gate stack is formed on top, with labels 156, 152, and 157 indicating different layers or regions. A central n-type region is labeled 'n'. Above the gate stack, there are various conductive and insulating layers, with labels 175, 176, 177, and 174 indicating different parts of the structure. The overall structure is more complex than the one shown in the main figure.

This diagram shows a cross-sectional view of a semiconductor device in the prior art. It features a substrate with a p-type region (152) and n+ regions (156, 157). A gate stack (175, 176, 177) is formed on top of the substrate. The gate stack consists of a gate oxide layer (175) and a gate electrode (176, 177). The gate electrode is formed by a layer of n+ material (156, 157) and a layer of p+ material (152). The gate oxide layer is formed by a layer of n+ material (156, 157) and a layer of p+ material (152). The gate electrode is formed by a layer of n+ material (156, 157) and a layer of p+ material (152). The gate oxide layer is formed by a layer of n+ material (156, 157) and a layer of p+ material (152).